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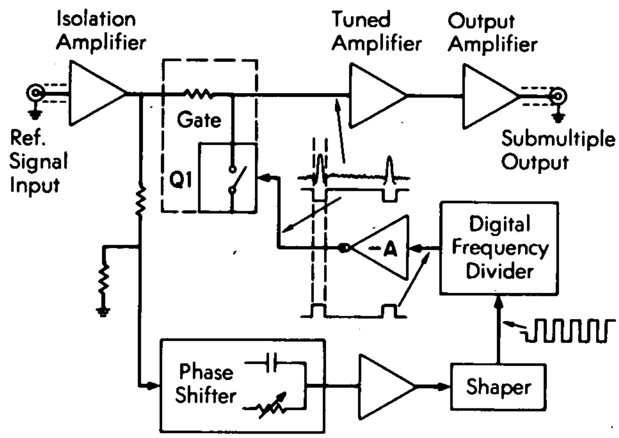
NASA TECH BRIEF

NASA Pasadena Office

Low Phase-Noise Digital Frequency Divider

The problem:

To minimize phase noise in the frequency-dividing circuits that are used in conjunction with atomic or maser frequency standards.



The solution:

A frequency dividing arrangement in which a digital divider and a gate are used in such a manner as to avoid the noise which characteristically occurs in other types of dividers. A digitally-generated countdown pulse at the submultiple frequency is applied to one electrode of an FET gate to establish a threshold state; the gate cannot function until the desired portion of the reference half-wave pulse which is to be passed appears on a second electrode.

How it's done:

As indicated in the diagram, a reference signal is introduced to the isolation amplifier and the amplified output is split; one portion is fed through a gate to a tuned amplifier, and the other portion is fed through a voltage divider to a phase-shift network.

The gate is essentially an FET transistor, Q1, operated as a switch. When the gate electrodes of Q1 are biased negatively, no current can flow between its source and drain and the device acts as a high impedance bypass on the output of the isolation amplifier; thus, signals coming from the amplifier pass to the tuned amplifier and thence to a broadband output amplifier. On the other hand, when the FET gate electrodes are biased positively, current can flow between source and drain, and the device presents a very low impedance to the output of the isolation amplifier, effectively short circuiting the output to ground.

The gate is controlled by an integrated circuit digital frequency divider set for any convenient division ratio which is a positive whole number. The fraction of the reference signal voltage coming from the phase shifter is amplified and then converted by a shaper into square waves of sufficient amplitude to drive the digital frequency divider module.

The output of the digital divider is a positive-going square wave, but since a negative-going keying signal is needed for operation of the gate, the digital frequency divider output is inverted by an amplifier at a voltage level sufficient to drive the FET gate transistor Q1. Ordinarily, noise from the digital divider and the gate appears in the vicinity of turn-on or turn-off. When gating is effected as shown in the diagram, noise cannot pass into the tuned amplifier because the keying pulse from the digital frequency divider is kept at a level which does not permit gate-transistor Q1 to open until the original reference signal positive half-wave crosses the zero axis in making

(continued overleaf)

the transition from negative to positive. During the interval defined by the negative-going portion of the keying square wave and the crossing of the zero axis by the reference signal, Q1 remains in the conducting state, shorting the reference signal output from the isolation amplifier. The gate transistor goes into cutoff only when the negative-going keying pulse is present on the gate electrode and the positive-going portion of the reference signal appears on the drain; thus, transistor Q1 is operated as an AND gate.

It is apparent that in passing through the various branches of the frequency dividing circuitry, the original signal will encounter different delays in each branch. The phase shifter establishes the time relationship between the particular cycle of the reference signal whose positive half-wave portion becomes the divided-down signal and the keying pulse at Q1. A variable resistor in the phase-shifting network makes possible the proper coincidence of the reference signal and the keying signal.

Notes:

1. The gating arrangement is capable of operating satisfactorily at input frequencies up to 10 MHz.
2. Requests for further information may be directed to:

   Technology Utilization Officer
   NASA Pasadena Office
   4800 Oak Grove Drive
   Pasadena, California 91103
   Reference: TSP 73-10135

Patent status:

This invention is owned by NASA, and a patent application has been filed. Inquiries concerning non-exclusive or exclusive license for its commercial development should be addressed to:

NASA Patent Counsel
Mail Code 1
NASA Pasadena Office
4800 Oak Grove Drive
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